WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a memory cell transistor provided on a semiconductor substrate; and

an access circuit for said memory cell provided on said substrate,

wherein said memory cell transistor includes a pair of memory electrodes of which one serves as a source electrode and the other serves as a drain electrode, and a channel region interposed between said pair of memory electrodes, said pair of memory electrodes and said channel region being provided in a first well region of said semiconductor substrate, and includes a first gate electrode disposed near said memory electrodes on said channel region with an insulating film interposed between said first gate electrode and said channel region, and a second gate electrode disposed on said channel region with an insulating film and a charge storage region interposed between said second gate electrode and said channel region and electrically isolated from said first gate electrode, and

wherein said access circuit is capable of selecting a first state in which a first negative voltage is applied to said first well region to thereby form a reverse-direction voltage applied state between said

second gate electrode and said memory electrode near said second gate electrode and to form an electric field for directing a first polarity charge from said well region side to said charge storage region, and a second state in which an electric field for directing a second polarity charge from said well region to said charge storage region is formed.

2. A semiconductor integrated circuit device according to claim 1,

wherein one first gate electrode is provided near one of said memory electrodes, and one second gate electrode and one charge storage region are respectively provided near the other thereof, and

wherein said memory cell transistor is capable of storing binary information according to a difference between an amount of said first polarity charge and an amount of said second polarity charge, each of which is injected into said charge storage region.

3. A semiconductor integrated circuit device according to claim 1,

wherein said second gate electrode and said charge storage region are provided near said memory electrode therefor, and one first gate electrode is provided in a region between a pair of said second gate electrodes, and

wherein said memory cell transistor is capable of

storing quaternary information according to a difference between an amount of a first polarity charge and an amount of a second polarity charge, each of which is injected into a pair of said charge storage regions.

4. A semiconductor integrated circuit device according to claim 3, wherein said access circuit is further capable of selecting a third state in which a current is allowed to flow from one memory electrode to the other memory electrode through said channel region, and a fourth state in which a current is allowed to flow from said other memory electrode to said one memory electrode through said channel region.

5. A semiconductor integrated circuit device comprising:

a memory cell transistor provided on a semiconductor substrate; and

an access circuit for said memory cell provided on said substrate,

wherein said memory cell transistor includes a pair of memory electrodes of which one serves as a source electrode and the other serves as a drain electrode, and a channel region interposed between said pair of memory electrodes, said pair of memory electrodes and said channel region being provided in a first well region of said semiconductor substrate, and includes a first gate

electrode disposed near one memory electrode on said channel region with an insulating film interposed between said first gate electrode and said channel region, and a second gate electrode disposed near the other memory electrode on said channel region with an insulating film and a charge storage region interposed between said second gate electrode and said channel region and electrically isolated from said first gate electrode, and

wherein said access circuit is capable of selecting a first state in which a first negative voltage is applied to said first well region to thereby apply a reverse voltage between said memory electrode near said second gate electrode and said first well region and to apply a voltage for forming an electric field for directing a first polarity charge from said well region side to said charge storage region to said second gate electrode, and a second state in which a voltage for forming an electric field for directing a second polarity charge to said charge storage region is applied to said second gate electrode and said first well region.

6. A semiconductor integrated circuit device according to claim 5,

wherein said access circuit has a first MIS transistor having a relatively thin gate insulating film, and a second MIS transistor having a relatively thick gate insulating film, and

wherein said access circuit sets a voltage applied to said memory electrode near said second gate electrode as a first operation power voltage of a circuit comprising said first MIS transistor in order to form said first state.

7. A semiconductor integrated circuit device according to claim 6, wherein said access circuit applies a second negative voltage smaller in absolute value than said first negative voltage to said first gate electrode when said first state is formed.

8. A semiconductor integrated circuit device according to claim 7, wherein said second negative voltage is a voltage substantially equal in absolute value to said first operation power voltage.

9. A semiconductor integrated circuit device according to claim 8, wherein said first negative voltage is a voltage substantially equal in absolute value to approximately several times said first operation power voltage.

10. A semiconductor integrated circuit device according to claim 5, wherein an electric field formed in said second state is an electric field for directing a second polarity charge from said well region to said

charge storage region.

11. A semiconductor integrated circuit device according to claim 10, wherein in said second state, a positive voltage is applied to said second gate electrode , and a circuit ground voltage is applied to said first well region.

12. A semiconductor integrated circuit device according to claim 11, wherein said circuit ground voltage is applied to said memory electrode near said second gate electrode in said second state.

13. A semiconductor integrated circuit device according to claim 9, wherein said access circuit is further capable of selecting a third state in which said second gate electrode is set to said circuit ground voltage, said first gate electrode is set to said first operation power voltage, and a current is allowed to flow in said channel region.

14. A semiconductor integrated circuit device according to claim 10, wherein hot holes are injected into said charge storage region in said first state, and electrons are injected into said charge storage region in said second state.

15. A semiconductor integrated circuit device according to claim 5, wherein said charge storage region is a nonconductive charge trap film.

16. A semiconductor integrated circuit device according to claim 5, wherein said charge storage region is an insulating film having conductive particles.

17. A semiconductor integrated circuit device according to claim 5, wherein said charge storage region is a conductive floating gate electrode covered with an insulating film.

18. A semiconductor integrated circuit device according to claim 5,

wherein said access circuit has a first MIS transistor having a relatively thin gate insulating film, and a MIS transistor having a relatively thick gate insulating film, and

wherein an insulating film for said first gate electrode is thinner than an insulating film for said second gate electrode.

19. A semiconductor integrated circuit device according to claim 18, wherein said insulating film for said first gate electrode is substantially equal to said gate insulating film of said first MIS transistor in

thickness.

20. A semiconductor integrated circuit device according to claim 19, further including a logic circuit connected to said access circuit and comprising said first MIS transistor.

21. A semiconductor integrated circuit device according to claim 20, wherein said logic circuit includes a CPU and a RAM.

22. A semiconductor integrated circuit device comprising:

a memory cell transistor provided on a semiconductor substrate; and

an access circuit for said memory cell provided on said substrate,

wherein said memory cell transistor includes a pair of memory electrodes of which one serves as a source electrode and the other serves as a drain electrode, and a channel region interposed between said pair of memory electrodes, said pair of memory electrodes and said channel region being provided in a first well region of said semiconductor substrate, and includes a first gate electrode disposed near a region for one memory electrode on said channel region with an insulating film interposed between said first gate electrode and said channel region,

and a second gate electrode disposed near a region for the other memory electrode on said channel region with an insulating film and a charge storage region interposed between said second gate electrode and said channel region and electrically isolated from said first gate electrode, and

wherein said access circuit is capable of selecting a first operation in which a negative voltage for forming a reverse bias state between said second gate electrode and said memory electrode near said second gate electrode is applied to said first well region to thereby inject a first polarity charge into said charge storage region, and a second operation in which a positive voltage is applied to said second gate electrode to thereby inject a second polarity charge into said charge storage region.

23. A semiconductor integrated circuit device according to claim 22,

wherein said access circuit has a first MIS transistor having a relatively thin gate insulating film, and a MIS transistor having a relatively thick gate insulating film, and

wherein said access circuit sets a voltage applied to said memory electrode near said second gate electrode as a first operation power voltage of a circuit comprising said first MIS transistor upon said first operation.

24. A semiconductor integrated circuit device according to claim 23, wherein said access circuit applies a second negative voltage smaller in absolute value than said first negative voltage to said first gate electrode upon said first operation.

25. A semiconductor integrated circuit device according to claim 24, wherein said second negative voltage is a voltage substantially equal to said first operation power voltage in absolute voltage.

26. A semiconductor integrated circuit device according to claim 25, wherein said first negative voltage is a voltage substantially equal to approximately several times said first operation power voltage in absolute value.

27. A semiconductor integrated circuit device according to claim 26, wherein said access circuit applies a second negative voltage larger than said first negative voltage in absolute value to said second gate electrode upon said first operation.

28. A semiconductor integrated circuit device according to claim 27, wherein said access circuit applies a circuit ground voltage to a well region upon

said second operation and applies said circuit ground voltage to said memory electrode near said second gate electrode.

29. A semiconductor integrated circuit device according to claim 26, wherein said access circuit is further capable of selecting a third operation in which said second gate electrode is set to said circuit ground voltage, said first gate electrode is set to said first operation power voltage, and a current is allowed to flow in said channel region.

30. A semiconductor integrated circuit device comprising:

a memory cell transistor;

a first MIS transistor relatively thin in gate insulating film; and

a second MIS transistor relatively thick in gate insulating film, said memory cell transistor, said first MIS transistor and said second MIS transistor being provided on a semiconductor substrate,

wherein said memory cell transistor includes a pair of memory electrodes of which one serves as a source electrode and the other serves as a drain electrode, and a channel region interposed between said pair of memory electrodes, said pair of memory electrodes and said channel region being provided in a first well region of

said semiconductor substrate, and includes a first gate electrode disposed near a region for one memory electrode on said channel region with an insulating film interposed between said first gate electrode and said channel region, and a second gate electrode disposed near a region for the other memory electrode on said channel region with an insulating film and a charge storage region interposed between said second gate electrode and said channel region and electrically isolated from said first gate electrode, and is capable of storing information different according to a difference between amounts of a first polarity charge and a second polarity charge injected into the charge storage region,

wherein said insulating film placed below the first gate electrode is substantially equal to said gate insulating film of said first MIS transistor in thickness,

wherein said well region is supplied with a negative voltage for forming a reverse bias state between said second gate electrode and said memory electrode near said second gate electrode when said first polarity charge is injected into said charge storage region, and

wherein said second gate electrode is supplied with a positive voltage when said second polarity charge is injected into said charge storage region.

31. A semiconductor integrated circuit device according to claim 30, wherein when said first polarity

charge is injected into said charge storage region, a first operation power voltage of a circuit comprising said first MIS transistor is applied to said memory electrode near said second gate electrode.

32. A semiconductor integrated circuit device according to claim 31, wherein when said first polarity charge is injected into said charge storage region, a second negative voltage smaller than said first negative voltage in absolute value is applied to said first gate electrode.

33. A semiconductor integrated circuit device according to claim 32, wherein said second negative voltage is a voltage substantially equal in absolute value to said first operation power voltage.

34. A semiconductor integrated circuit device according to claim 33, wherein said first negative voltage is a voltage substantially equal in absolute value to approximately several times said first operation power voltage.

35. A semiconductor integrated circuit device according to claim 34, wherein when said first polarity charge is injected into said charge storage region, a second negative voltage larger than first negative

voltage in absolute value is applied to said second gate electrode.

36. A semiconductor integrated circuit device according to claim 35, wherein when said second polarity charge is injected into said charge storage region, a circuit ground voltage is applied to the well region, and said circuit ground voltage is applied to said memory electrode near said second gate electrode.

37. A semiconductor integrated circuit device according to claim 34, wherein when said memory information of said memory cell transistor is read, said circuit ground voltage is applied to said second gate electrode and said first operation power voltage is applied to said first gate electrode to bring about a state in which a current is allowed to flow in said channel region.

38. A semiconductor integrated circuit device comprising:

a memory cell transistor provided on a semiconductor substrate; and

an access circuit for said memory cell provided on said substrate,

wherein said memory cell transistor includes a pair of memory electrodes of which one serves as a source

electrode and the other serves as a drain electrode, and a channel region interposed between said pair of memory electrodes, said pair of memory electrodes and said channel region being provided in a first well region of said semiconductor substrate, and includes, over said channel region, memory gate electrodes separately disposed near said respective memory electrodes through insulating films and charge storage regions, and a control gate electrode disposed between both said memory gate electrodes with an insulating film interposed therebetween and electrically isolated from said memory gate electrodes, and

wherein said access circuit is capable of selecting a first state in which a negative voltage is applied to the first well region to form a reverse bias state between said well region and said one memory electrode and to form an electric field for directing a first polarity charge from said well region side to said charge storage region on said one memory electrode side, a second state in which an electric field for directing a second polarity charge from said well region to said charge storage regions of both said memory gate electrodes is formed, and a third state in which a current is allowed to mutually flow from said one memory electrode to said other memory electrode through said channel region.

39. A semiconductor integrated circuit device comprising:

a memory cell transistor provided on a semiconductor substrate; and

an access circuit for said memory cell provided on said substrate,

wherein said memory cell transistor includes a pair of memory electrodes of which one serves as a source electrode and the other serves as a drain electrode, and a channel region interposed between said pair of memory electrodes, said pair of memory electrodes and said channel region being provided in a first well region of said semiconductor substrate and includes, over said channel region, memory gate electrodes separately disposed near said respective memory electrodes through insulating films and charge storage regions, and a control gate electrode disposed between both said memory gate electrodes with an insulating film interposed therebetween and electrically isolated from said memory gate electrodes, and

wherein said access circuit is capable of selecting a first operation in which a negative voltage is applied to said first well region to thereby form a reverse bias state between said first well region and said one memory electrode and inject a first polarity charge into said one charge storage region, a second operation in which a positive voltage is applied to both said memory gate

electrodes to thereby inject a second polarity charge from said well region to both said charge storage regions, and a third operation in which a current is allowed to mutually flow from said one memory electrode to said other memory electrode through said channel region.

40. A semiconductor integrated circuit device comprising:

a memory cell transistor;

a first MIS transistor relatively thin in gate insulating film; and

a second MIS transistor relatively thick in gate insulating film, said memory cell transistor, said first MIS transistor and said second MIS transistor being provided on a semiconductor substrate,

wherein said memory cell transistor includes a source region, a drain region and a channel region interposed between said source region and said drain region, which are provided within a first well region of said semiconductor substrate, and includes a first gate electrode disposed on one sides of the source region and drain region, a second gate electrode disposed on the other sides of said source region and drain region, a first gate insulating film formed between said channel region and said first gate electrode, a charge storage region formed between said channel region and said second gate electrode, and an insulating film for electrically

isolating said first gate electrode from said second gate electrode, which are provided over said channel region, and

wherein upon a write or erase operation of the memory cell transistor, a negative voltage having a value smaller in absolute value than one equal to several times a power voltage of a circuit comprising said first MIS transistor, and a ground voltage for said circuit are applied to said first well region to thereby inject carriers into said charge storage region.

41. A semiconductor integrated circuit device according to claim 40, wherein upon said write or erase operation of said memory cell transistor, a negative first voltage is applied to said second gate electrode and a negative second voltage smaller than said negative first voltage in absolute value is applied to said first gate electrode to thereby inject holes into said charge storage region.

42. A semiconductor integrated circuit device comprising:

a memory cell transistor,

wherein said memory cell transistor includes a source region, a drain region, and a channel region interposed between said source region and the drain region, which are provided within a first well region of

a semiconductor substrate, and includes a first gate electrode, a second gate electrode, a first gate insulating film formed between said channel region and said first gate electrode, a charge storage region formed between said channel region and said second gate electrode, and an insulating film for electrically isolating said first gate electrode from said second gate electrode, which are provided over said channel region, and

wherein upon a write or erase operation of the memory cell transistor, a negative first voltage is applied to said second gate electrode and a negative second voltage smaller than said negative first voltage in absolute value is applied to said first gate electrode to thereby inject holes into said charge storage region.

43. A semiconductor integrated circuit device according to claim 40,

wherein said first gate electrode is electrically connected to a first driver circuit for driving a gate control line, through said gate control line,

wherein said first driver circuit comprises a low withstand voltage transistor, and

wherein said first gate insulating film is formed in a gate insulating film forming process for said low withstand voltage transistor.

44. A semiconductor integrated circuit device according to claim 40,

wherein said charge storage region comprises a nonconductive charge trap film,

wherein said charge storage region is formed over said channel region with a first insulating film interposed therebetween,

wherein said first gate electrode constitutes a control gate electrode, and

wherein said second gate electrode constitutes a memory gate electrode.

45. A semiconductor integrated circuit device comprising:

a memory cell transistor;

a first MIS transistor relatively thin in gate insulating film; and

a second MIS transistor relatively thick in gate insulating film, said memory cell transistor, said first MIS transistor and said second MIS transistor being provided on a semiconductor substrate,

wherein said memory cell transistor includes a source region, a drain region, a channel region interposed between said source region and said drain region, a gate electrode, and a charge storage region formed between said channel region and said gate electrode, which are provided within a first well region

of said semiconductor substrate, and

wherein upon a write or erase operation of said memory cell transistor, a negative first voltage is applied to said gate electrode, a negative second voltage not greater than the first voltage in absolute value is applied to said first well region, and a third voltage not greater in absolute value than a power voltage of a circuit comprised of said first MIS transistor is applied to said source or drain region to thereby inject holes into said charge storage region.

46. A semiconductor integrated circuit device according to claim 45, wherein upon said write or erase operation of said memory cell transistor, a difference in potential between said third voltage and said second voltage is close to a junction withstand voltage of said source or drain region and is capable of generating holes by band-to-band tunneling.

47. A semiconductor integrated circuit device according to claim 45,

wherein said source region or said drain region is electrically connected to a first driver circuit for driving a bit control line, through said bit control line,

wherein said first driver circuit comprises a low withstand voltage transistor,

wherein said charge storage region is comprised of

a nonconductive charge trap film, and

wherein said charge storage region is formed over said channel region with a first insulating film interposed therebetween.

48. A semiconductor integrated circuit device comprising:

a memory cell transistor; and

a peripheral circuit transistor,

wherein said memory cell transistor includes, in a memory cell forming region of a semiconductor substrate, a source region, a drain region, a channel region interposed between said source region and said drain region, a first gate electrode and a second gate electrode disposed on said channel region, a first gate insulating film formed between said channel region and said first gate electrode, a charge storage region formed between said channel region and said second gate electrode, and an insulating film for electrically isolating said first gate electrode from said second gate electrode,

wherein said peripheral circuit transistor has a gate electrode over a peripheral circuit transistor forming region of said semiconductor substrate, and

wherein said gate electrode of said peripheral circuit transistor comprises a film formed by laminating a first conductive film lying in the same layer as said

first gate electrode, and a second conductive film lying in the same layer as said second gate electrode.

49. A semiconductor integrated circuit device according to claim 48,

wherein said charge storage region comprises a nonconductive charge trap film,

wherein said first gate electrode constitutes said control gate electrode,

wherein said second gate electrode constitutes a memory gate electrode and is formed on side walls of said control gate electrode through an insulating film in sidewall spacer fashion, and

wherein said second conductive film is formed on said first conductive film.

50. A semiconductor integrated circuit device according to claim 48, wherein said peripheral transistor includes a low withstand voltage transistor operated at a power voltage, and a high withstand voltage transistor operated at a voltage higher than said power voltage.

51. A semiconductor integrated circuit device according to claim 50, wherein said first gate insulating film is formed by a gate insulating film forming process for said low withstand voltage transistor.

52. A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

forming a first conductive film over a memory cell forming region and a peripheral circuit transistor forming region of a semiconductor substrate;

patterning said first conductive film lying over the memory cell forming region to form a first conductive pattern which serves as a first gate electrode of a memory cell and leaving said first conductive film over said peripheral circuit transistor forming region;

forming a second conductive film over said memory cell forming region and said first conductive film in said peripheral circuit transistor forming region; and

etching said second conductive film to form each second gate electrode of said memory cell on at least side walls of said first conductive pattern, and forming a gate electrode of each peripheral circuit transistor comprising said second conductive film and first conductive film over said peripheral circuit transistor forming region.

53. A method according to claim 52,

wherein said memory cell includes, in a memory cell forming region of said semiconductor substrate, a source region, a drain region, a channel region interposed between said source region and said drain region, a control gate electrode and a memory gate electrode

disposed over said channel region, a first gate insulating film formed between said channel region and said control gate electrode, and a charge storage region formed between said channel region and said memory gate electrode,

wherein said first gate electrode constitutes said control gate electrode, and

wherein said second gate electrode constitutes said memory gate electrode.

54. A method according to claim 53,

wherein said peripheral circuit transistors include a low withstand voltage transistor operated at a power voltage, and a high withstand voltage transistor operated at a voltage higher than said power voltage, and

wherein said first gate insulating film is formed in a gate insulating film forming step for said low withstand voltage transistor.

55. A method according to claim 53, wherein said second gate electrode is formed on side walls of said first gate electrode through an insulating film in sidewall spacer fashion.

56. A method according to claim 53, wherein an electrode withdrawal portion of said second gate electrode is formed in said forming step of the second

gate electrode.

57. A method according to claim 53, further including a step of patterning said first conductive pattern after said formation of the second gate electrode to thereby form said first gate electrode.

58. A semiconductor integrated circuit device comprising:

a memory cell,

wherein said memory cell includes a source region, a drain region, and a channel region interposed between said source region and said drain region, which are provided within a semiconductor region, and includes a first gate electrode, a second gate electrode, and an insulating film for electrically isolating said first gate electrode from said second gate electrode, which are provided over said channel region,

wherein said channel region comprises a first channel region and a second channel region,

wherein a first gate insulating film is provided between said first channel region and said first gate electrode,

wherein a second gate insulating film is provided between said second channel region and said second gate electrode,

wherein said second gate electrode is formed higher

than said first gate electrode, and

wherein a silicide layer for said second gate electrode and a silicide layer for said first gate electrode are electrically isolated by sidewall spacers, each comprised of an insulating film, which are formed in self-alignment with side walls of said second gate electrode.

59. A semiconductor integrated circuit device comprising:

a memory cell,

wherein said memory cell includes a source region, a drain region, and a channel region interposed between said source region and said drain region, which are provided within a semiconductor region, and includes a first gate electrode, a second gate electrode, and an insulating film for electrically isolating said first gate electrode from said second gate electrode, which are provided over said channel region,

wherein said channel region comprises a first channel region and a second channel region,

wherein a first gate insulating film is provided between said first channel region and said first gate electrode,

wherein a second gate insulating film is provided between said second channel region and said second gate electrode,

wherein said second gate electrode is formed on side walls of the first gate electrode through an insulating film in sidewall spacer form,

wherein a thickness of said second gate electrode is thicker than a thickness of said first gate electrode, and

wherein a height on a substrate surface, of said second gate electrode is higher than a height on said substrate surface, of said first gate electrode.

60. A semiconductor integrated circuit device according to claim 59, wherein a silicide layer is formed in said second gate electrode.

61. A semiconductor integrated circuit device according to claim 58,

wherein sidewall spacers each comprised of an insulating film formed in self-alignment with side walls on both sides of the second gate electrode,

wherein said silicide layer for said second gate electrode and said silicide layer for said first gate electrode are electrically isolated by said sidewall spacer disposed on one side of both sides,

wherein said silicide layer for said second gate electrode and a silicide layer for said source region or said drain region are electrically isolated by said sidewall spacer on the other side thereof, and

wherein said silicide layer for said first gate electrode and said silicide layer for said source region or said drain region are electrically isolated by sidewall spacers, each comprised of an insulating film, which are formed in self-alignment with said sidewalls of said first gate electrode.

62. A semiconductor integrated circuit device according to claim 58,

wherein said second gate insulating film includes a nonconductive charge trap film corresponding to a charge storage region,

wherein said first gate electrode constitutes a control gate electrode of said memory cell, and

wherein said second gate electrode constitutes a memory gate electrode of said memory cell and is formed on side walls of said control gate electrode through an insulating film in sidewall spacer fashion.

63. A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

forming a first conductive film over a memory cell forming region of a semiconductor substrate and forming an insulating film over said first conductive film;

etching said insulating film and said first conductive film to form a first conductive pattern which serves as a first gate electrode of a memory cell;

forming a second gate electrode of said memory cell on side walls of said first conductive pattern;

removing said insulating film over said first conductive pattern;

forming sidewall spacers, each comprised of an insulating film, in self-alignment with side walls of said second gate electrode; and

forming a silicide layer for each of said first conductive pattern and said second gate electrode in self-alignment with respect to said sidewall spacers.

64. A method according to claim 63,

wherein in said sidewall spacer forming step, said sidewall spacers are formed on said side walls on both sides of said second gate electrode and side walls of said first gate electrode,

wherein said silicide layer for said second gate electrode and said silicide layer for said first gate electrode are electrically isolated by said sidewall spacer disposed on one side of said both sides,

wherein said silicide layer for said second gate electrode and a silicide layer for a source region or a drain region are electrically isolated by said sidewall spacer on the other side thereof, and

wherein said silicide layer for said first gate electrode and said silicide layer for said source region or said drain region are electrically isolated by

sidewall spacers formed on said side walls of said first gate electrode.

65. A method according to claim 63, wherein a gate electrode of each peripheral circuit transistor is formed of a film obtained by laminating a conductive film lying in the same layer as said first conductive film, and a second conductive film lying in the same layer as said memory gate electrode.

66. A method according to claim 63,

wherein sidewall spacers are formed on side walls of said gate electrode of the peripheral circuit transistor in said sidewall spacer forming step, and

wherein a silicide layer is formed over said gate electrode of said peripheral circuit transistor in said silicide layer forming step.

67. A method according to claim 63,

wherein said memory cell includes, in a memory cell forming region of a semiconductor substrate, a source region, a drain region, a channel region interposed between said source region and said drain region, a control gate electrode disposed near one of said source and drain regions, a memory gate electrode disposed near the other of said source and drain regions, a first gate insulating film formed between said channel region and

said control gate electrode, and a charge storage region formed between said channel region and said memory gate electrode,

wherein said first gate electrode constitutes said control gate electrode, and

wherein said second gate electrode constitutes said memory gate electrode.

68. A semiconductor integrated circuit device comprising:

a memory cell,

wherein said memory cell includes a source region, a drain region, and a channel region interposed between said source region and said drain region, which are provided within a semiconductor region, and includes a first gate electrode, a second gate electrode, and an insulating film for electrically isolating said first gate electrode from said second gate electrode, which are provided over said channel region,

wherein said channel region comprises a first channel region and a second channel region,

wherein a first gate insulating film is provided between said first channel region and said first gate electrode,

wherein a second gate insulating film is provided between said second channel region and said second gate electrode,

wherein said second gate electrode is formed higher than said first gate electrode, and

wherein said first gate electrode is formed in self-alignment with respect to sidewall spacers, each comprised of an insulating film, formed in self-alignment with respective side walls of said second gate electrode.

69. A semiconductor integrated circuit device according to claim 68,

wherein sidewall spacers each comprising an insulating film, are formed in self-alignment with said side walls of said second gate electrode,

wherein said second gate insulating film is formed in self-alignment with respect to said sidewall spacer on one side of said both sides, and

wherein said first gate electrode is formed in self-alignment with respect to said sidewall spacer on the other side thereof.

70. A semiconductor integrated circuit device according to claim 68,

wherein said second gate insulating film includes a nonconductive charge trap film corresponding to a charge storage region,

wherein said first gate electrode constitutes a control gate electrode, and

wherein said second gate electrode constitutes a

memory gate electrode and is formed on side walls of said control gate electrode through an insulating film in sidewall spacer fashion.

71. A method of manufacturing a semiconductor integrated circuit device, comprising steps of:

forming a first conductive film over a memory cell forming region of a semiconductor substrate and forming an insulating film on said first conductive film;

etching said insulating film and said first conductive film to form a first conductive pattern which serves as a first gate electrode of a memory cell;

forming a second gate electrode of said memory cell on side walls of said first conductive pattern;

removing said insulating film over said first conductive pattern;

forming sidewall spacers, each comprised of an insulating film, in self-alignment with side walls of said second gate electrode; and

etching said first conductive pattern in self-alignment with respect to said sidewall spacers to form corresponding first gate electrode.

72. A method according to claim 71,

wherein a second gate insulating film is formed between said second gate electrode and said semiconductor substrate,

wherein said sidewall spacers are formed on said side walls on both sides of said second gate electrode,

wherein said second gate insulating film is formed in self-alignment with respect to said sidewall spacer on one side of said both sides, and

wherein said first gate electrode is formed in self-alignment with respect to said sidewall spacer on the other side thereof.

73. A method according to claim 71, wherein a gate electrode of each peripheral circuit transistor is formed of a film obtained by laminating a conductive film lying in the same layer as said first conductive film, and a second conductive film lying in the same layer as said memory gate electrode.

74. A method according to claim 71,

wherein said second gate insulating film includes a nonconductive charge trap film corresponding to a charge storage region,

wherein said first gate electrode constitutes a control gate electrode, and

wherein said second gate electrode constitutes a memory gate electrode and is formed on side walls of said control gate electrode through an insulating film in sidewall spacer fashion.

75. A semiconductor integrated circuit device comprising:

a memory cell transistor provided on a semiconductor substrate; and

an access circuit for said memory cell provided on said substrate,

wherein said memory cell transistor includes a pair of memory electrodes of which one serves as a source electrode and the other serves as a drain electrode, and a channel region interposed between said pair of memory electrodes, said pair of memory electrodes and said channel region being provided in a first well region of said semiconductor substrate and includes, over said channel region, a first gate electrode disposed near said corresponding memory electrode with an insulating film interposed between said first gate electrode and said channel region, and a second gate electrode disposed on said channel region with an insulating film and a charge storage region interposed between said second gate electrode and said channel region and electrically isolated from said first gate electrode, and

wherein said access circuit is capable of selecting a first state in which a first negative voltage is applied to said first well region to thereby form a reverse voltage applied state between said second gate electrode and said memory electrode near said second gate electrode and form an electric field for directing a

first polarity charge from said well region side to said charge storage region.

76. A semiconductor integrated circuit device comprising:

a memory cell transistor provided on a semiconductor substrate; and

an access circuit for said memory cell provided on said substrate,

wherein said memory cell transistor includes a pair of memory electrodes of which one serves as a source electrode and the other serves as a drain electrode, and a channel region interposed between said pair of memory electrodes, said pair of memory electrodes and said channel region being provided in a first well region of said semiconductor substrate and includes, over the channel region, a first gate electrode disposed near said one memory electrode with an insulating film interposed between said channel region and said first gate electrode, and a second gate electrode disposed near the other memory electrode on said channel region with an insulating film and a charge storage region interposed between said second gate electrode and said channel region and electrically isolated from said first gate electrode, and

wherein said access circuit is capable of selecting a first state in which a first negative voltage is

applied to said first well region to thereby apply a reverse voltage between said memory electrode near said second gate electrode and said first well region and apply to said second gate electrode a voltage for forming an electric field for directing a first polarity charge from said well region side to said charge storage region.

77. A semiconductor integrated circuit device according to claim 1, wherein in said first state, a state of application of a reverse voltage near or greater than or equal to a junction withstand voltage is formed between said memory electrode near said second gate electrode and said first well region.

78. A semiconductor integrated circuit device comprising:

a memory cell transistor provided on a semiconductor substrate; and

an access circuit for said memory cell provided on said substrate,

wherein said memory cell transistor includes a pair of memory electrodes of which one serves as a source electrode and the other serves as a drain electrode, and a channel region interposed between said pair of memory electrodes, said pair of memory electrodes and said channel region being provided in a first well region of said semiconductor substrate and includes, over said

channel region, a first gate electrode disposed near a region for said one memory electrode with an insulating film interposed between said first gate electrode and said channel region, and a second gate electrode disposed near a region for the other memory electrode on said channel region with an insulating film and a charge storage region interposed between said second gate electrode and said channel region and electrically isolated from said first gate electrode, and

wherein said access circuit is capable of selecting a first operation in which a negative voltage for forming a state of a reverse bias greater than or equal to a junction withstand voltage between said second gate electrode and said memory electrode near said second gate electrode is applied to said first well region to thereby inject a first polarity charge into said charge storage region.

79. A semiconductor integrated circuit device comprising:

a memory cell transistor;

a first MIS transistor relatively thin in gate insulating film; and

a second MIS transistor relatively thick in gate insulating film, said memory cell transistor, said first MIS transistor and said second MIS transistor being provided on a semiconductor substrate,

wherein said memory cell transistor includes a pair of memory electrodes of which one serves as a source electrode and the other serves as a drain electrode, and a channel region interposed between said pair of memory electrodes, said pair of memory electrodes and said channel region being provided in a first well region of said semiconductor substrate and includes, over said channel region, a first gate electrode disposed near a region for said one memory electrode with an insulating film interposed between said first gate electrode and said channel region, and a second gate electrode disposed near a region for the other memory electrode on said channel region with an insulating film and a charge storage region interposed between said second gate electrode and said channel region and electrically isolated from said first gate electrode, and is capable of storing information different according to a difference between amounts of a first polarity charge and a second polarity charge injected into said charge storage region,

wherein said insulating film placed below said first gate electrode is substantially equal to said gate insulating film of said first MIS transistor in thickness, and

wherein said well region is supplied with a negative voltage for forming a reverse bias state between said second gate electrode and said memory electrode near

said second gate electrode when said first polarity charge is injected into said charge storage region.

80. A semiconductor integrated circuit device comprising:

a memory cell transistor provided on a semiconductor substrate; and

an access circuit for said memory cell provided on said substrate,

wherein said memory cell transistor includes a pair of memory electrodes of which one serves as a source electrode and the other serves as a drain electrode, and a channel region interposed between said pair of memory electrodes, said pair of memory electrodes and said channel region being provided in a first well region of said semiconductor substrate and includes, over said channel region, memory gate electrodes separately disposed near the respective memory electrodes through insulating films and charge storage regions, and a control gate electrode disposed between both said memory gate electrodes with insulating films interposed therebetween and electrically isolated from said memory gate electrodes, and

wherein said access circuit is capable of selecting a first state in which a negative voltage is applied to said first well region to thereby form a reverse bias state between said first well region and said one memory

electrode and form an electric field for directing a first polarity charge from said well region side to the charge storage region on said corresponding one memory electrode side, and a third state in which a current is allowed to mutually flow from said one memory electrode to the other memory electrode through said channel region.

81. A semiconductor integrated circuit device comprising:

a memory cell transistor provided on a semiconductor substrate; and

an access circuit for said memory cell provided on said substrate,

wherein said memory cell transistor includes a pair of memory electrodes of which one serves as a source electrode and the other serves as a drain electrode, and a channel region interposed between said pair of memory electrodes, said pair of memory electrodes and said channel region being provided in a first well region of said semiconductor substrate and includes, over said channel region, memory gate electrodes separately disposed near said respective memory electrodes through insulating films and charge storage regions, and a control gate electrode disposed between both said memory gate electrodes with insulating films interposed therebetween and electrically isolated from said memory gate electrodes, and

wherein said access circuit is capable of selecting a first operation in which a negative voltage is applied to said first well region to thereby form a reverse bias state between said first well region and said one memory electrode and inject a first polarity charge into said one charge storage region, and a third operation in which a current is allowed to mutually flow from said one memory electrode to the other memory electrode through said channel region.

82. A semiconductor integrated circuit device according to claim 22, wherein in said first operation, a state of a reverse voltage bias near or greater than or equal to a junction withstand voltage is formed between said memory electrode near said second gate electrode and said first well region.

83. A semiconductor integrated circuit device comprising:

a memory cell transistor provided on a semiconductor substrate; and

an access memory for said memory cell provided on said substrate,

wherein said memory cell transistor includes a pair of memory electrodes of which one serves as a source electrode and the other serves as a drain electrode, and a channel region interposed between said pair of memory

electrodes, said pair of memory electrodes and said channel region being provided in a first well region of said semiconductor substrate and includes, over said channel region, a first gate electrode disposed near said corresponding memory electrode with a first gate insulating film interposed therebetween, and a second gate electrode disposed through a second gate insulating film and a charge storage region and electrically isolated from said first gate electrode, and

wherein said first gate electrode is different in conductivity type from said second gate electrode.

84. A semiconductor integrated circuit device according to claim 83, wherein said first gate insulating film is different in thickness from said second gate insulating film.

85. A semiconductor integrated circuit device according to claim 84, wherein a thickness of said first gate insulating film is thinner than a thickness of said second gate insulating film, said first gate electrode is a p type, and said second gate electrode is an n type.